Temperature Dependence of Fowler–Nordheim Current in 6H- and 4H-SiC MOS Capacitors

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***Abstract*—This work reports on Fowler–Nordheim (F–N) injection studies on n-type 6H-SiC and 4H-SiC MOS systems under positive gate bias from 25 to 325 °C. At a given temperature and electric field, the current density in the 4H-SiC MOS system is about five times higher than that in 6H-SiC due to the smaller effective barrier height for the 4H-SiC MOS system as compared to 6H-SiC. The reduction of the effective barrier height with temperature, particularly in 4H-SiC, raises serious concerns about the long-term reliability of gate oxides in SiC. It is concluded that the maximum practical values of electric field in the 4H-SiC MOS system under positive gate bias and high junction temperature should be reduced to below the values used in the Si MOS system.**

THE STUDY of the temperature dependence of Fowler–Nordheim (F–N) current in SiC Metal-Oxide-Semiconductor (MOS) devices is of considerable interest because it limits the high-field, high-temperature performance of MOS-based power devices such as power MOS Field-Effect-Transistors (MOSFET's), Insulated-Gate-Bipolar-Transistors (IGBT's) and MOS-Controlled-Thyristors (MCT's). The large band-gaps of 6H-SiC (2.85 eV) and 4H-SiC (3.26 eV) result in negligible leakage currents even at temperatures as high as 400 °C and make them ideal candidates for power devices. Operation at high junction temperature should simplify cooling requirements, resulting in considerable savings in systems weight and cost. Analysis of the SiC vertical power MOSFET, ignoring the limitations imposed by F–N injection of free carriers into the gate oxide, has yielded extremely attractive performance estimates [1]. However, it is well known from extensive research on Si MOS devices that the combination of high electric field and high temperature promotes F–N injection-induced time-dependent dielectric breakdown (TDDB) of gate oxides [2]. Thus, it is reasonable to expect that SiC power MOS devices will also be limited by F–N injection. In fact, the F–N injection is expected to be enhanced in SiC MOS system due to smaller barrier heights. This represents a serious limitation of SiC power MOS devices and requires an urgent consideration.

A schematic cross section of a vertical *U*-groove power MOSFET (UMOSFET) structure in SiC is shown in Fig. 1. Under the steady-state on-condition, the source is grounded, the gate voltage is at its maximum positive value and the drain

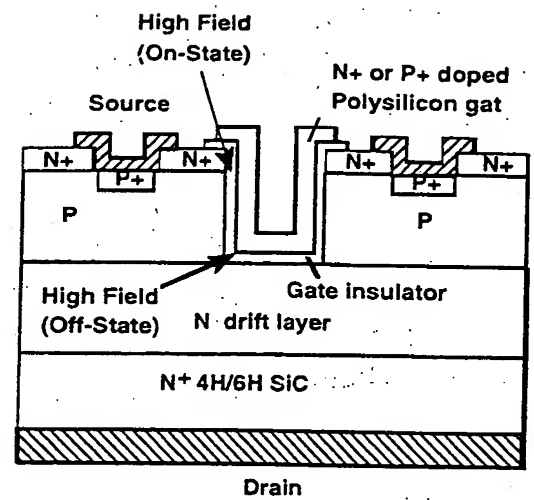

Fig. 1. A schematic cross section of a vertical power UMOSFET structure illustrating high electric field regions under on and off states.

voltage is approximately 3 V. A high electric field is induced in the insulator overlapping the N$^+$ source regions due to the application of high gate bias which induces electron injection from N$^+$ SiC into the gate oxide. The barrier controlling the F–N injection of electrons is measured from the conduction band edge of SiC to the conduction band edge of silicon dioxide. This barrier is shown in Fig. 2 for Si, 6H-SiC and 4H-SiC as established from room temperature F–N measurements and internal photo-emission studies [3], [4]. It is evident that the 4H-SiC/SiO_2 system has the lowest barrier height and is therefore expected to have the highest F–N injection at a given electric field. This is unfortunate as 4H-SiC is the material of choice because of its four to five times higher electron mobility along the *c*-axis (direction of current flow in vertical devices) as compared to 6H-SiC [5]. At elevated temperatures, the F–N current increases due to temperature induced statistical spreading in the carrier energy. The broadening of the electron distribution allows a larger fraction of electrons to tunnel through the thinner (upper) part of the triangular barrier. This phenomenon is well understood in Si MOS devices [6]. Recently, F–N injection studies at elevated temperatures on 6H-SiC MOS capacitors were reported [7]. It was found that the effective barrier height for electrons in 6H-SiC decreases from room temperature value of 2.95 eV to about 2 eV at 327 °C. The effective barrier height in 4H-SiC/SiO_2 system is expected to be even lower at elevated temperatures. The reduction of effective barrier height at higher operating temperatures raises serious concerns about the long-term reliability –

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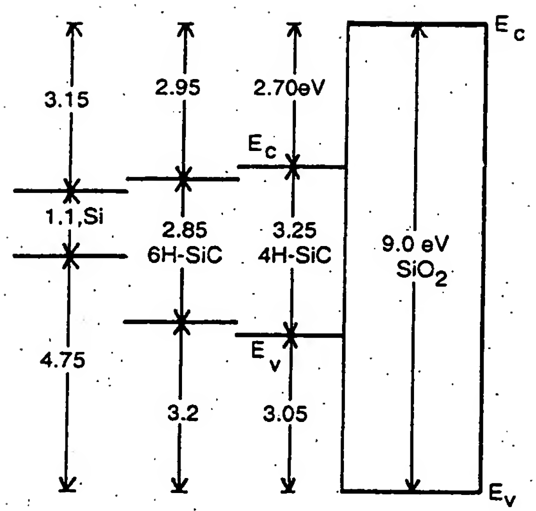

Fig. 2. Energy band diagrams of Si, 6H-SiC, 4H-SiC, and SiO_2 illustrating barrier heights for F–N electron injection from semiconductor into the gate oxide [3], [4].

of SiC MOS devices. Thus, a maximum limit on the electric field under the on-condition of the power MOSFET structures should be established for a given junction temperature and given projected lifetime of the device. This maximum electric field will limit the inversion charge and hence the specific on-resistance of the power MOSFET. In this letter, we report on our results on F–N injection from N-type 6H- and 4H-SiC from room temperature to 325 °C.

MOS capacitors were fabricated on n-type 6H- and 4H-SiC epitaxial layers grown on the Si face of N^+ 6H- and 4H-SiC substrates oriented 3.5° off (0001). The 2-μm thick epitaxial layers were doped with nitrogen resulting in a doping density of 1×10^{17} cm^{-3}. The substrate doping was n-type with a doping density of 2×10^{18} cm^{-3}. The wafers were cleaned in two steps. First, the epitaxial layers were subjected to ozone and ultraviolet radiation in order to remove carbon from the surface [8]. Next, the samples received the standard RCA clean. A sacrificial oxide was formed at 1050 °C with the pyrogenic technique for 6 h and stripped in buffered HF solution. The preoxidation ozone and RCA cleans were repeated and the final oxide was formed in dry oxygen at 1050 °C for 16 h followed by a 1.5 h argon anneal. This resulted in about 260 and 225 Å thick thermal oxide layers on the silicon face of the 6H-SiC and 4H-SiC, respectively. A 315 Å film of silicon nitride film was then deposited by low-pressure chemical vapor deposition at 775 °C. The nitride film does not have any effect on the SiC/SiO_2 barrier height or shape for electric field exceeding 1.2 MV/cm. The nitride and oxide layers were removed from the back of the wafers by reactive ion etching. Ni was sputtered and sintered in forming gas at 800 °C for 2 min. Metal dots of 100 μm diameter consisting of 500 Å of Ti, 1500 Å of Pt, and 4000 Å of gold were evaporated on the frontside followed by a 1 h forming gas anneal at 450 °C.

The equivalent oxide thickness including the nitride film was determined on each device by measuring capacitance at 1 MHz with the capacitor biased well into accumulation. The destructive current–voltage ($I-V$) measurements were carried out by stepping the gate bias from zero to positive values

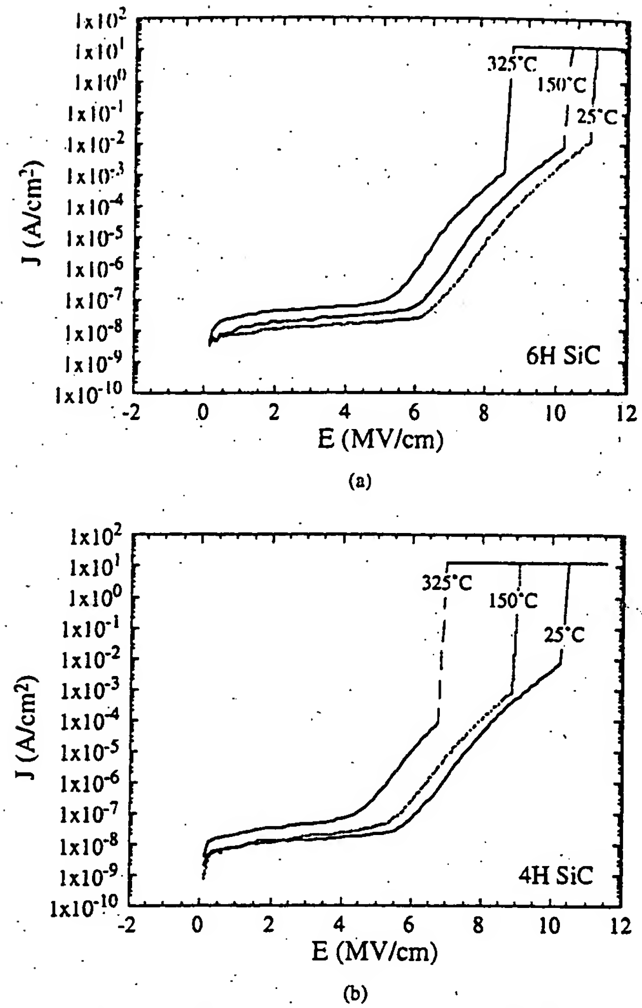

Fig. 3. Plot of current density versus electric field measured at different temperatures on oxides grown in dry oxygen on 6H- and 4H-SiC (n-type) under positive gate bias.

with respect to the n-SiC, thus injecting electrons from the conduction band of SiC into the gate insulator. Knowing the area of the gate electrode and equivalent oxide thickness, the current-voltage data were converted into a current density vs. electric field plot (shown in Fig. 3) for 6H- and 4H-SiC at three different temperatures. Several observations can be made from the data in Fig. 3: 1) The dielectric breakdown field strength for both 6H- and 4H-SiC MOS systems at room temperature is between 10 and 11 MV/cm; 2) as temperature is increased to 325 °C, the dielectric strength reduces to about 6.5 MV/cm for 4H-SiC whereas it stays relatively high at 8.5 MV/cm for 6H-SiC, and 3) at a given temperature and electric field, the current density in 4H-SiC MOS system is about five times higher than that in 6H-SiC. This difference may be explained by the smaller room temperature effective barrier height for the 4H-SiC MOS system as compared to the 6H-SiC. Thus, with respect to the dielectric strength at elevated temperatures, thermal oxides grown on 6H-SiC in dry oxygen seem to be superior to those grown on 4H-SiC.

Fig. 4 shows F–N plots for the two MOS systems for different temperatures. Data for Si from [6] are also shown for comparison. The linear behavior over three decades of current

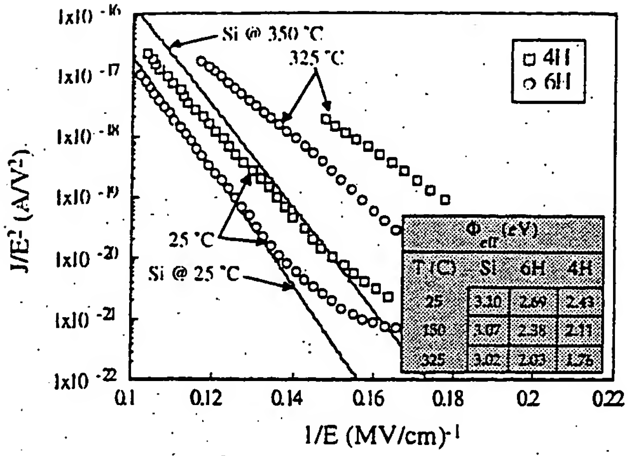

Fig. 4. F–N plots of electron injection at different temperatures in dry oxides grown on 6H- and 4H- SiC (n-type) under positive gate bias. Also shown, for comparison, is data for silicon from [6].

density demonstrates that the conduction is indeed determined by F–N tunneling. The effective barrier height (Φ_b) at the SiC-oxide interface was evaluated by regression using the classical expression for F–N tunneling

$$J_{\mathrm{FN}}(T) = A(T)E_{\mathrm{ox}}^2 \exp\left(-\frac{B(T)}{E_{\mathrm{ox}}}\right),$$
$$A(T) = \frac{q^3 m_{\mathrm{SiC}}}{8\pi h m_{\mathrm{ox}} \Phi_b}, \quad B(T) = \frac{4\sqrt{2m_{\mathrm{ox}}\Phi_b^3}}{3q\hbar}$$

where q is the electron charge, m_{SiC} and m_{ox} are the effective electron mass in the SiC and SiO_2, respectively, $h(\hbar)$ is the (reduced) Planck constant, E_{ox} is the electric field in the oxide and Φ_b is the effective barrier height in eV measured from the SiC conduction band to the oxide conduction band. The value of m_{ox} was taken to be $0.42m_{\mathrm{Si}}$ [9]. The value of m_{SiC} is not needed as $B(T)$ is used to extract the effective barrier height. However, a good set of values for the effective mass in 6H-SiC can be found in [10]. The extracted barrier heights at different temperatures for 6H, 4H-SiC and Si are shown in the inset of Fig. 4. The room temperature values for 6H- and 4H-SiC agree reasonably well with those shown in Fig. 2. It should be noted that the effective barrier height Φ_b, extracted from F–N measurements at high electric fields, is always lower than the actual barrier height. The extracted values of Φ_b for 6H-SiC at different temperatures match well with the values in [7]. The effective barrier height at elevated temperature is much lower than the room temperature value for both 6H-SiC, and 4H-SiC whereas the effective barrier height in silicon remains relatively constant up to 350 °C. This raises serious concerns about the reliability of SiC power MOS devices operating at elevated temperatures. In order to determine a maximum limit on the electric field across the gate oxide in 4H-SiC MOS system, long term TDDB measurements are needed. However, it is clear that the maximum electric field in the 4H-SiC MOS system should be much lower than the value used for silicon. It should be reduced further for operation at higher junction temperatures. This would adversely impact the on-resistance of the inversion layer.

There is a more serious issue under negative gate bias with respect to SiC where F–N injection of electrons may occur from the gate electrode into the oxide film. In order to minimize this injection, gate electrode material with a high work function such as P^+ doped polysilicon should be chosen. Even then, the field in the oxide may have to be limited to approximately 4 MV/cm. This limits the maximum field in SiC ($E_{\mathrm{SiC}} = E_{\mathrm{ox}}\epsilon_{\mathrm{ox}}/\epsilon_{\mathrm{SiC}}$, neglecting any charges at the SiC/SiO_2 interface) under negative bias to about 1.6 MV/cm, well below the SiC breakdown field of 3 MV/cm. This would reduce the breakdown voltage of the SiC power devices for a given thickness and doping density of the drift layer. It is, therefore, concluded that the electrical performance SiC power MOSFET devices, (on-resistance, transconductance, breakdown voltage, etc.) will be limited by the reliability of the gate oxide under high electric field and high temperature and not by the electronic properties of SiC. The case for other insulators such as silicon nitride or Ta_2O_5 with high dielectric constants needs to be examined in this light, although the smaller barrier heights in these materials may negate the advantage of higher dielectric constant. Other power devices, such as MOS Turn-Off Thyristor (MTO), where the gate oxide is shielded from the high field regions may also prove to be more reliable [11].

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